

**EXHIBIT A**

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

1        151. (Amended) A synchronous memory device including an array  
2 of memory cells, the synchronous memory device comprises:

3        clock receiver circuitry to receive an external clock signal;

4        input receiver circuitry to sample a first operation code  
5 [synchronously with respect] in response to a rising edge  
6 transition of the external clock signal;

7        a programmable register to store a value which is  
8 representative of an amount of time to transpire before the memory  
9 device outputs data, wherein the memory device stores the value in  
10 the programmable register in response to the first operation code;  
11 and

12       output driver circuitry to output data in response to a second  
13 operation code, wherein the data is output after the amount of time  
14 transpires, and wherein:

15           the output driver circuitry outputs a first portion of  
16 the data synchronously with respect to a rising edge  
17 transition of the external clock signal and outputs a second  
18 portion of the data synchronously with respect to a falling  
19 edge transition of the external clock signal.

1        154. (Amended) The memory device of claim 151 wherein the  
2 memory device is a synchronous dynamic random access memory [DRAM].

1        155. (Amended) The memory device of claim 151 wherein the  
2 input receiver circuitry receives the second operation code and  
3 address information [corresponding to at least one memory cell  
4 location of the array of memory cells].

1        156. (Amended) The memory device of claim 155 [151] wherein  
2 the input receiver circuitry receives [at least one of] the second  
3 operation code and the address information on consecutive clock  
4 cycles of the external clock signal [corresponding to at least one  
5 memory cell location of the array of memory cells].

1        157. (Amended) The memory device of claim 151 wherein the  
2 amount of time is [representative of] a number of clock cycles of  
3 the external clock signal.

1        159. (Amended) The memory device of claim 158 wherein the  
2 input receiver circuitry receives the third operation code and  
3 address information [corresponding to at least one memory cell  
4 location of the array of memory cells].

1        160. (Amended) The memory device of claim 151 further  
2 including delay lock loop circuitry coupled to the clock receiver  
3 circuitry to generate a first internal clock signal, wherein the  
4 data is output in response to [using] the first internal clock  
5 signal.

1        162. (Amended) The memory device of claim 161 wherein the bus  
2 includes a set of signal lines [used] to carry [transmit]  
3 multiplexed address information, data and control information.

1        163. (Amended) A method of operation of a synchronous memory  
2 device, wherein the memory device includes an array of memory cells  
3 and a programmable register, the method of operation of the memory  
4 device comprises:

5        sampling a first operation code synchronously with respect to  
6 an external clock signal;

7        receiving a binary value which is representative of an amount  
8 of time to transpire before the memory device outputs data in  
9 response to a second operation code wherein the memory device  
10 stores the binary value in the programmable register in response to  
11 the first operation code [wherein the binary value is  
12 representative of an amount of time to transpire before the memory  
13 device outputs data in response to a second operation code];

14        sampling the second operation code; and

15        outputting the data after the amount of time transpires,  
16 wherein a first portion of the data is output synchronously with  
17 respect to a first transition of the external clock signal and a  
18 second portion of the data is output synchronously with respect to  
19 a second transition of the external clock signal.

1        174. (Amended) The method of claim 163 wherein the memory  
2 device [samples the first operation code from an external bus, and  
3 wherein the memory device] outputs the data onto an [the] external  
4 bus.

1        175. (Amended) The method of claim 174 wherein the external  
2 bus includes a set of signal lines [used] to carry [transmit]  
3 multiplexed address information, data and control information.

1        176. (Amended) A method of controlling a synchronous memory  
2 device by a memory controller, wherein the memory device includes  
3 an array of memory cells and a programmable register, the method of  
4 controlling the memory device comprises:

5        providing [issuing] a first operation code to the memory  
6 device, wherein the first operation code initiates an access of the  
7 programmable register in the memory device in order to store a  
8 binary value;

9        providing the binary value to the memory device, wherein the  
10 memory device stores the binary value in the programmable register  
11 in response to the first operation code;

12        providing [issuing] a second operation code to the memory  
13 device, wherein the second operation code instructs the memory  
14 device to accept data that is issued by the memory controller;

15        providing [issuing] a first portion of the data to the memory  
16 device [synchronously with respect to a first] in response to a  
17 rising edge transition of the external clock signal; and

18        providing [issuing] a second portion of the data to the memory

19 device [synchronously with respect to a second] in response to a  
20 falling edge transition of the external clock signal.

1 177. (Amended) The method of claim 176 wherein the binary  
2 value is representative of a delay time to transpire before the  
3 memory device samples the data, and wherein the first portion of  
4 the data is [issued] provided to the memory device after the delay  
5 time transpires.

1 178. (Amended) The method of claim 176 wherein the binary  
2 value is representative of a number of clock cycles of the external  
3 clock signal to transpire before the memory device samples the  
4 data, and wherein the first portion of the data is provided to the  
5 memory device after the delay time transpires.

1 179. (Amended) The method of claim 176 wherein the binary  
2 value is representative of a delay time to transpire before the  
3 memory device outputs data in response to an operation code which  
4 instructs the memory device to output data[the first transition of  
5 the external clock signal is a rising edge transition and the  
6 second transition of the external clock signal is a falling edge  
7 transition].

1 183. (Amended) The method of claim 176 wherein the first  
2 operation code and the data are [issued onto] provided to the  
3 memory device via an external bus.

1        184. (Amended) The method of claim 183 wherein the external  
2 bus includes a set of signal lines used to carry [transmit]  
3 multiplexed address information, the data and control information.

1        186. (Amended) A synchronous memory device, wherein the memory  
2 device includes an array of memory cells, the memory device  
3 comprises:

4        input receiver circuitry to sample a first operation code  
5 [synchronously with respect] in response to a first transition of  
6 an external clock signal;

7        a programmable register to store a binary value in response to  
8 the first operation code, wherein the binary value is  
9 representative of an amount of time to transpire before the memory  
10 device outputs data; and

11       output driver circuitry to output data in response to a second  
12 operation code and after the amount of time transpires, wherein a  
13 first portion of the data is output [synchronously with respect] in  
14 response to a second [first] transition of the external clock  
15 signal and a second portion of the data is output [synchronously  
16 with respect] in response to a third [second] transition of the  
17 external clock signal.

1        [188. The memory device of claim 187 wherein the binary value  
2 is representative of a fractional number of clock cycles of the  
3 external clock signal.]

1        188. (Amended) The memory device of claim 186 wherein the  
2        [first] second transition of the external clock signal is a rising  
3        edge transition and the [second] third transition of the external  
4        clock signal is a falling edge transition.

1        189. (Amended) The memory device of claim 188 wherein the  
2        [first and] second and third transitions of the external clock  
3        signal are consecutive transitions.

1        192. (Amended) The memory device of claim 186 further  
2        including delay lock loop circuitry to generate a first internal  
3        clock signal, wherein the data is output [using] in response to the  
4        first internal clock signal.

1        193. (Amended) The memory device of claim 186 wherein the  
2        input receiver circuitry receives address information  
3        [corresponding to at least one memory cell location of the array of  
4        memory cells].

1        194. (Amended) The memory device of claim 186 wherein the  
2        output driver circuitry outputs the data onto an external bus  
3        having a set of signal lines used to [transmit] carry multiplexed  
4        address information, the data and control information.

1        197. (Amended) The memory device of claim 186 wherein the  
2        memory device is a synchronous dynamic random access memory [DRAM].